In the Specification:

Please substitute the following paragraphs for the corresponding paragraphs beginning at the indicated location in the specification as originally filed.

In the Title of the Application:

Please change the Title of the application at all occurrences to:

"AN INSTRUCTION BUFFER AND METHOD OF CONTROLLING THE INSTRUCTION BUFFER WHERE BUFFER ENTRIES ARE ISSUED IN A PREDETERMINED ORDER"

Page 6, line 15+:

The instruction registering stage 4 includes a ~~ROB~~ registration order buffer (ROB) 21, an operation instruction buffer 22, and a memory access instruction buffer 23. the ROB 21 is connected to the instruction decoders 15 through decode register 18 of the instruction decoding stage 3. The ROB 21 sequentially registers all instructions in order of input and sequentially releases them in order of completion. The ROB 21 stores the order of instructions and is used to detect the dependence of on each other and to confirm the completion of instructions. The operation instructions are registered at the operation instruction buffer 22 and then issued, as will be described specifically later. The memory access instructions are registered at the memory access instruction buffer 23 and then issued, as will also be described specifically later.

Page 13, line 13+:

FIGS. 7A through ~~7A~~ 7C demonstrate how the illustrative embodiment issues an operation instruction while executing the buffer queue control. As shown in FIG. 7A, at the timing T1, the operation instructions ALU-1 through ALU-3 are registered at the entries #61

through #63, respectively. The other entries #64 through #66 are idle. The operation instruction ALU-1 is shown as being issued to the instruction issue register 24 by way of example. As shown in Figure 7B, at the timing T2, the entry #61 is idle. As shown in Figure 7C, at the timing T3, the operation instructions ALU-2 and ALU-3 are shifted to the entries #61 and #62, respectively, while the operation instruction ALU-2 is issued to the instruction issue register 24. In this manner, the illustrative embodiment issues an operation instruction while executing the buffer queue control.

Page 16, line 8+:

Assume that the memory access instruction MEM-1 ~~has~~ is dependent on the operation instruction ALU-3 and should be issued after the instruction ALU-3. Also, assume that ~~that~~ the memory access instruction MEM-2 is dependent on the operation instruction ALU-4 and should be issued after the instruction ALU-4. Further, assume that the memory access instruction MEM-3 is dependent on the operation instruction ALU-5 and should be issued after the instruction ALU-5.

Page 16, line 17+:

FIG. 10 is a timing chart showing the conditions of the memory access instructions MEM-1 through MEM-3 and operation instructions ALU-3 through ALU-8 registered as shown in FIG. 9. In FIG. 10, alphabets R, AI, AX and AW respectively denote the instruction registering stage 4, instruction issuing stage 5, instruction executing stage 6, and instruction completing stage 7. Likewise alphabets ~~E1, EX~~ EI, EE and EW respectively denote the instruction issuing stage 5, instruction executing stage 6, and instruction completing stage 7.

Page 17, line 2+:

The memory access instructions MEM-1 through MEM-3 each have dependence ~~each~~ and are therefore not issued unless the dependence cancellation report 32 is output. In addition, the instructions MEM-1 through MEM-3 are sequentially issued in order of entry number in buffer 23. The operation instructions ALU-3 through ALU-8 do not have dependence and are therefore sequentially issued in order of entry number in buffer 22.

Page 20, line 12+:

FIG. 13 is a timing chart demonstrating how the memory access instructions MEM-1 through MEM-3 and operation instructions ALU-3 through ALU-8, registered as shown in FIG. 12, are dealt with. Briefly, the memory access instructions MEM-1 through MEM-3 each have dependence and are therefore not issued unless the dependence cancellation report 32 is output. In addition, the instructions MEM-1 through MEM-3 are sequentially issued in order of entry number in buffer 23. The operation instructions ALU-3 through ALU-8 have no dependence and are therefore sequentially issued in order of entry number in buffer 22.